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ANALYSIS AND DESIGN OF A NEW STRUCTURE FOR 10-BIT 350MS/S PIPELINE ANALOG TO DIGITAL CONVERTER

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Abstract: A 10-bit pipelined Analog to Digital converter is proposed in this paper with using 0.18 µm TSMC technology. In this paper, a new structure is proposed to increase the speed of the pipeline analog to digital convertor. So at the first stage is not used the amplifier and instead the buffer is used for data transfer to the second stage. The speed of this converter is 350MS/s. An amplifier circuit with accurate gain of 6 and a very accurate unit gain buffer circuit that are open loop with a new structure were used. In this Converter, the first 3 bits are extracted simultaneously with sampling. The proposed analog-to-digital converter was designed with the total power consumption 75mW using power supply of 1.8v.

Keywords: Analog to Digital Pipeline, Comparator, Amplifiers, Buffer

Introduction

Today Analog signals have been replaced by digital signals. Analog-to-digital convertor (ADC) play a key role in today's modern telecommunications [1-5].So far, various structures have been proposed for the implementation of analog-to-digital converters, which have different specifications. One of these structures is pipeline analog to digital converter. The purpose of this design is to improve speed.

In this structure, there is an amplifier as well as a sample and hold circuit between the blocks of each stage. At the end of each cycle, part of the digital output code is extracted and an extra signal is transferred to the next block. The speed of this structure is independent of the number of stages used. This structure, like other sub-ranging structures, can achieve high precision using low hardware [6-15].As a result, the output

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of all comparators whose reference voltage is smaller than the sampled signal is one, and vice versa the output of all comparators whose reference voltage is larger than the sampled signal is zero. Given that these comparisons are performed in a completely parallel manner, and the speed of this type of convertor depends only on the comparators or the sampler circuit, the flash analogue to digital convertor can have very high speeds. But the two major problems with this structure are the sensitivity of the comparators to the offset input and a lot of hardware has been used in it, because, as mentioned, it requires 2^{n-1} comparator. On the other hand a many number of comparators increase the scale and power consumption. Therefore, a convertor with this structure requires high levels and high power to achieve high precision. Hence, these structures are not actually used to build 10-bit convertor s because they cost more and require high power consumption and more space. Another structure used is the Two Step flash convertor. The basic block of this convertor is the same type of flash convertor. This structure is made up of two successive flash memory modules [16-17]. The mode of operation of this type of convertor is such that on the first floor, the bits of the signal are detected. Then a digital-to-analog convertor returns the equivalent of the analog bits of value. This amount is reduced from the original signal value and the remainder enters the second stage. In this stage, low-value bits are extracted. Obviously, the conversion time for this convertor is long as compared with the simple flash type convertor, but instead uses a smaller number of comparators, which means less than $2^{n/2}\times2$ comparators. By breaking the conversion process to several steps, the number of comparators is reduced. But the conversion time increases. The Subranging converter has several processing steps, which are specified by the number of stages [18-21]. Structures, it is necessary to have a structure that has very high speed and acceptable power consumption.

In reference [1], a 10-bit ADC is proposed with a power consumption of 19.7mW, which has a low speed of 100MS/s, voltage supply is 1.8v in 0.18µm technology, In Reference [1], for design 10-bit Pipeline Analog to Digital it used two-stage, and has used two flashes (3bits and 4bits) at each stage but in this 10-bit Pipeline Analog to Digital proposed we used one flashes (just 4bits) at each stage, on the stage1 is not used the gain stage, Instead, it used buffer, That's an advantage and makes the power consumption decreases and the converter speed increases, On the other hand to speed up on the stage2 we used open loop amplifier, also comparator designed is able to eliminate unwanted offsets and detect the smallest amount of input. In reference [2], pipeline ADC is designed with a low speed and high power consumption of 136mW, in other hand, the voltage supply is high. In

reference [17], a 10-bit ADC is proposed with a speed of 50MS/s using 0.13µm technology, which has a low speed, but the figure of merit is not good. A 14-bit ADC with a 1GS/s speed is presented in 65nm technology at [22], and it has SNR 69dB and the SFDR 86 dB, but it has a high power consumption of 1200mW. In [23], a 14-bit ADC is proposed with a speed of 500MS/s, voltage supply is 1.8v in 0.18µm technology, which has high power consumption of 950mW. A 12-bit ADC is proposed in [24], voltage supply is 1.2v in 0.065µm technology, which has a speed of 250MS/s and power consumption of 49.7mW. In reference [25], a 14-bit ADC with a speed of 250MS/s in 0.18µm technology is proposed which has an acceptable speed, but has a high power consumption of 120mW.In [26], a 9-bit ADC with a speed of 50MS/s and figure of merit -437dB in 0.18µm technology is proposed, which has a low speed and a high power consumption of 65mW. In reference [27], an 8-bit ADC is proposed with a speed of 166MS/s and figure of merit -421dB in 0.18µm technology, which has a low speed and high power consumption of 38.9mW, but the figure of merit is not good. In reference [28], a 10-bit ADC with a speed of 125/250MS/s dual in 0.18µm technology is proposed, which has an acceptable speed, but has a high power consumption of 32mW. This study is divided into 4 sections. In Section 1, the block diagram of the proposed pipeline convertor is presented, and in the second section, the design of various ADC convertor circuits is examined. In Section 3, the simulation results of different blocks are presented and finally in Section 4, a general comparison is made between the proposed design and several references published in recent years.

1. Proposed Pipeline Convertor

Since the pipeline ADC is suitable for applications that require high precision and high bandwidth [27-30]. Given that the present study tends to determine an ADC design with sampling speed of 350 MS/s and due to the high speed of information conversion and the use of a channel to reach the target (parallelization is not working), the pipeline structure is used. This ADC consists of consecutive stages, each of which is responsible for extracting a number of digital signal bit output. Each of these stages includes ADCs with lower bits, DACs, subtracter and amplifier to amplify the remaining signal. Obviously, only an ADC is used in the final stage.

According to the studies conducted, it is necessary to have an extremely low power and very fast processing speed ADC. Also, the proposed design must occupy the lowest area and can provide a trade-off between speed and power consumption, to open the designer's hand for

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various applications. The general proposed block diagram is shown in Figure1

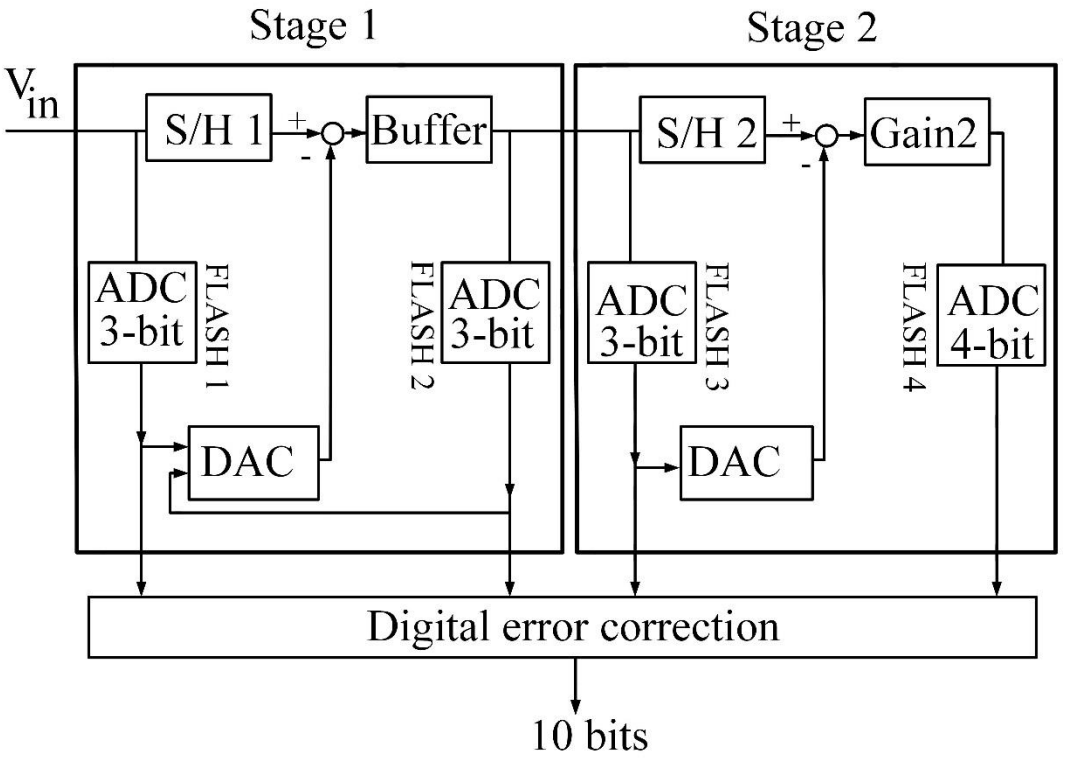

Figure 1. Block diagram of the proposed 10-bit pipeline A/D convertor

Since in pipeline analog to digital convertor is disappears about half of conversion time in the amplifier, So As shown in Figure1, on the stage1 is not used the amplifier, Instead, it used buffer, That's an advantage and makes the power consumption decreases and the convertor speed increases, but the circuit of the buffer must have a high precision and high speed, So that it can transfer data quickly to the next stage. Therefore on the stage2, the comparator's performance will be very difficult because the signal reached to this stage is not amplified, comparator must be able to eliminate unwanted offsets and detect the smallest amount of input In other words, the comparator should be very precise and it have to can recognize difference between very small voltages. Also an open loop amplifier is designed to further increase the convertor speed at stage2. A new error correction circuit was designed for the Ring Counter. Since it is necessary for a 10-bit Pipeline Analog to Digital

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convertor to have the S/H circuit having a minimum accuracy of 11 bits. Therefore, the S/H circuit designed has a precision above 11 bits.

Due to the fact that in this study tends to determine an ADC design with a precision of 10 bits and a sampling rate of 350 MS/s, at this rate of conversion, the time available for each conversion is equal to 2.5 ns. About 50% of the time is considered for Sample and Hold. For the remainder of the time, a portion of it is consumed to perform the comparison and generate the code. Also, a part is used to convert the digitalized data from the first stage to the analogue. In the proposed structure, most of the circuits have been innovated, and as much as possible, extra bits of the input data are extracted. The total time available for each conversion is 2.5 ns, with a duration of 1 ns divided into S/H. This is shown in Figure 2.

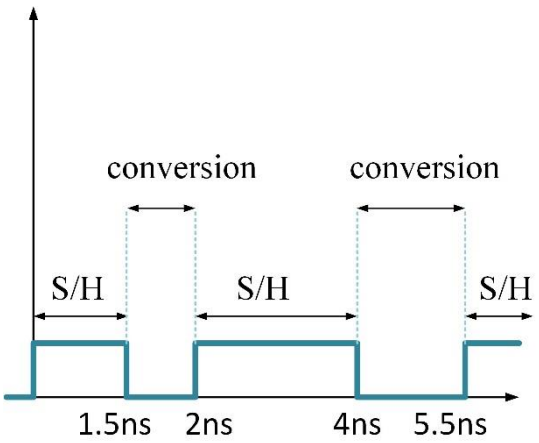

Figure 2. Allocations of scheduling to the proposed convertor

Simultaneously with the completion of Sampling, we allow the comparators of first stage to perform the comparison. At time of 1.5 ns, the binary data of the first stage is generated, and the amount of the analogue or level of this stage is also prepared to subtract the original signal. After reducing the data extracted from the first stage input data, an open loop buffer that has a high speed to transmit data to the next stage is required. The designed buffer, which will be explained in the next section, has this speed and precision ratio of 1. Since there is no amplification from this stage to the next stage, we used the comparators with higher precision in the next stage.

As we know, by a comparator circuit with n-bit precision we can extract a maximum of n bit digits from an input signal. Therefore, good ADCs (with high precision) require high precision comparator circuits. By using the error correction algorithm in the converters, high precision ADCs can be implemented with lower accuracy comparator circuits. The error resulting from each stage is corrected by the extracted bits in the next stage. In this case, in order to correct the error in the ADC output, we need to add and subtract the operator. In this paper, we use method of reference [1], To make the correction easier, we increased the comparison levels by 1/2 LSB. Therefore, raising the comparison levels for error correction caused to we need only summation. If an error occurs in a comparison in the ADC pipeline, the residue value is strengthened to the extent that it can be detected in the next category by the comparator circuitry of the next classes. The amount of amplified residue is reached to a degree that it can be detected in the next stage by comparison circuits of the next stages. The extracted bit is summed with the bit extracted by the error, and the error is corrected.

2. Block circuit design

The first part of the design section of the ADC is the design of the S/H block. When the high accuracy S/H at the entrance could not be designed, in the subsequent steps nothing could be done with the corrupted data. The use of Active S/H requires a Pomp, which has 2 major weaknesses. The first weakness in this type of S/H is the high power consumption dissipated by the Pomp. The second weakness is the Pomp's limited bandwidth. Due to the limited time in this study, limited Pomp bandwidth did not allow the use of active S/H. Therefore, we used the S/H passive. According to errors associated with ADC, the required accuracy S/H must be at least 11-bit, to attain a 10-bit pipeline ADC. The proposed circuit is shown in Figure 3.

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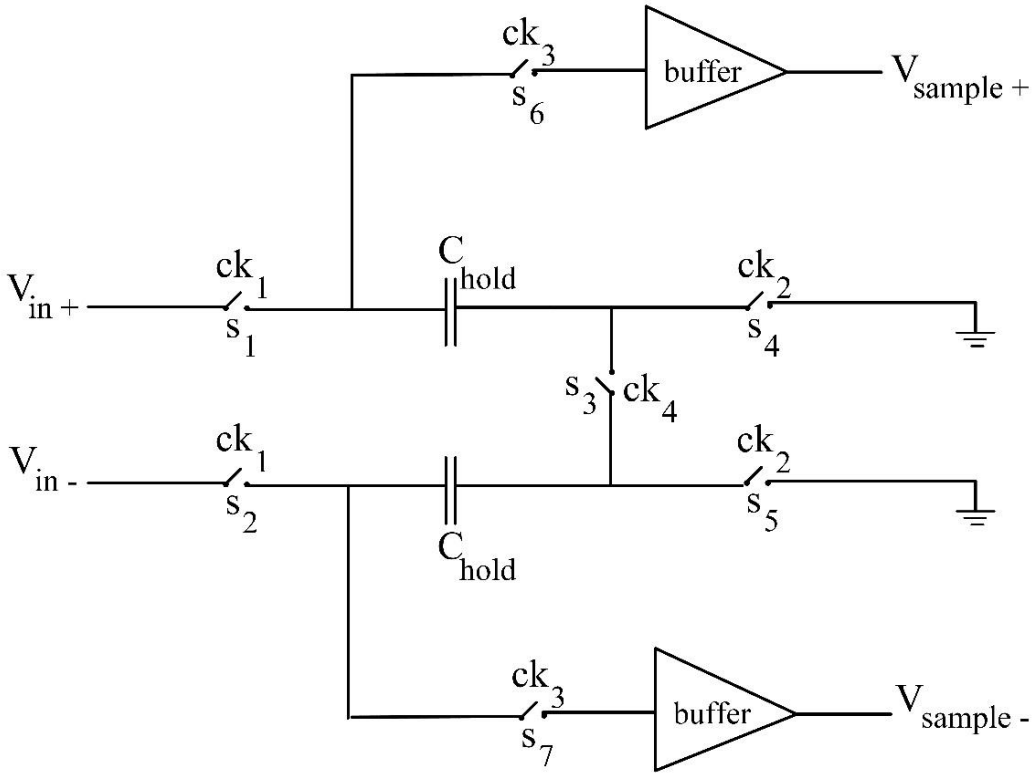

Figure 3. Proposed S/H structure

Also, because analog voltage goes straight to the S/H in the first stage and requires a precision of 7 bits, the capacitor is 0.2 PF, and the second stage requires a precision of 8 bits, in which we used a capacitor of 0.8 PF [31].

For switches, NMOS or PMOS transistors can be used depending on the amount of common mode input. If we assume that the input CM has a value close to zero, we can use NMOS. This is because with zero CM voltage, there will be no errors or some kind of offset in the circuit, and the circuit will operate in a perfectly symmetrical manner.

For sampling, the first S_3 key is opened and the information is stored in the capacitors. As a result, the sampling procedure is solved with three keys (or the NMOS transistor). After opening the S_3 key, as shown in Figure 4, the charge channel of the transistor inputs is expected to flow to the input due to the path open to the sample capacitors. This does not spoil the Sample information on the capacitors.

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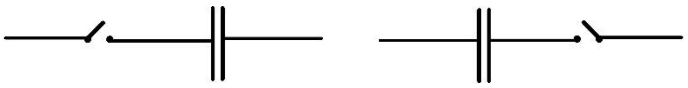

Figure 4. Open path to release transistor channel charge

But in the S/H pseudo structure, one of the problems faced with is the effect of loading the next stage. This effect flushes out the circuit output on the charge of the sampler capacitors and corrupts the data. To avoid this, as shown in Figure 3, buffer is used in the two outlets. The used buffer which is linearly acceptable should have a high bias current and use larger size transistors. The consequence of adding a buffer to the S/H output node is to add significant amounts of parasitic capacitance to the output nodes. The destructive effect of these parasitic capacitors will be on the S/H circuit function. After opening the S_3 key, the path is not open to sampling capacitors, and thus the channel charge can pass through this path and distort the sampled data.

The recent solution to this problem is as follows: Something should be done to remove the parasitic capacitor in the input buffer from output node of S/H when the S_3 key is opening. The path to the sampling capacitors completely opens after the S_3 key opens and as such, the charge of the channel cannot pass through the sampler capacitors.

To achieve this, we put two small switches into the buffer input path. These switches are always ON according to the timing of the clocks shown in Figure 5 and will only open in a small interval from the time before the S_3 key is opened and after opening, the S_1 and S_2 keys are closed.

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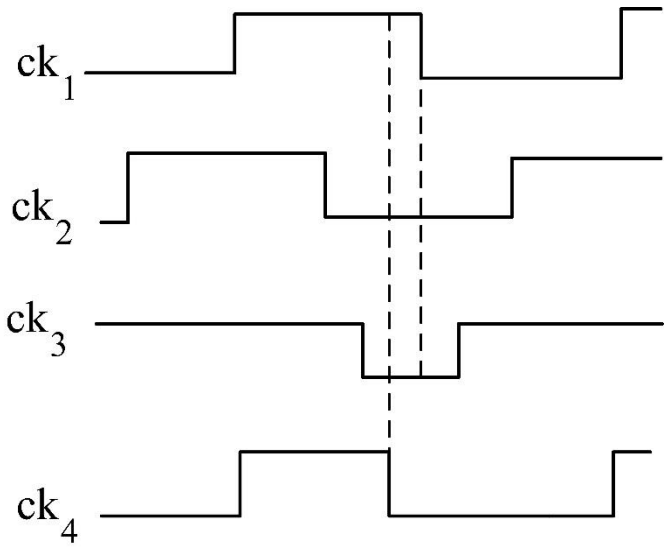

Figure 5. Schedule suggested S/H keys

2.1. Comparator

After sampling the input information in the Flash convertor, comparators are needed to compare the input information with different voltage levels and make the corresponding binary output corresponds to it. As soon as the differential circuit name comes up, this circuit amplifies the difference between two signals; therefore, it seems logical that a comparator can be made using a differential amplifier. One of the important design problems is the lack of full compliance with the elements used in these circuits so that the input information can be detected incorrectly. Another issue faced in the design of comparator is the limited gain of the circuit. This problem reveals its impact when there is little difference between input information and reference information. When this difference is low, the output signal is also small and cannot be detected. To compensate for this problem, we use a latch class in the comparator circuit output so that we can make even the small signal in the output of the circuit to convey identified information to the next digital block. This structure is shown in Figure 6.

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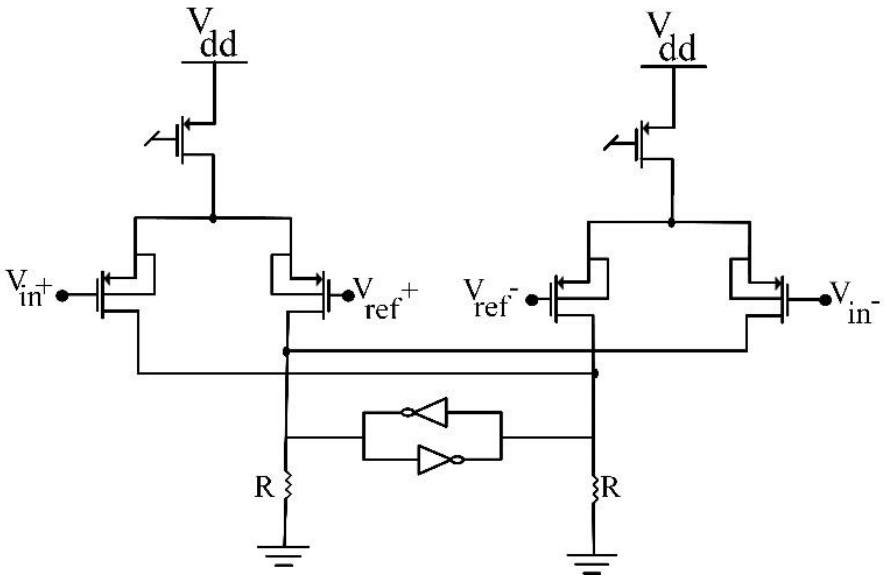

Figure 6. The first Proposed Comparator Structure.

Also, we put a switch on the two ends of the Latch output. So, by the time we want to identify the information, first, by closing this switch, the previous information must have been cleared in a word and the Latch circuit can work properly. After putting Latch on the output, we are faced with the problem of Kick back noise. In cases where the input range is small, it can be destroyed. To solve this problem, the common practice is to use a Pre-amplifier stage to convert a low-input signal to a better-suited signal and then deliver it to the Latch circuit on the next stage. In this study, the structure of Figure 7 for the comparator circuit is used.

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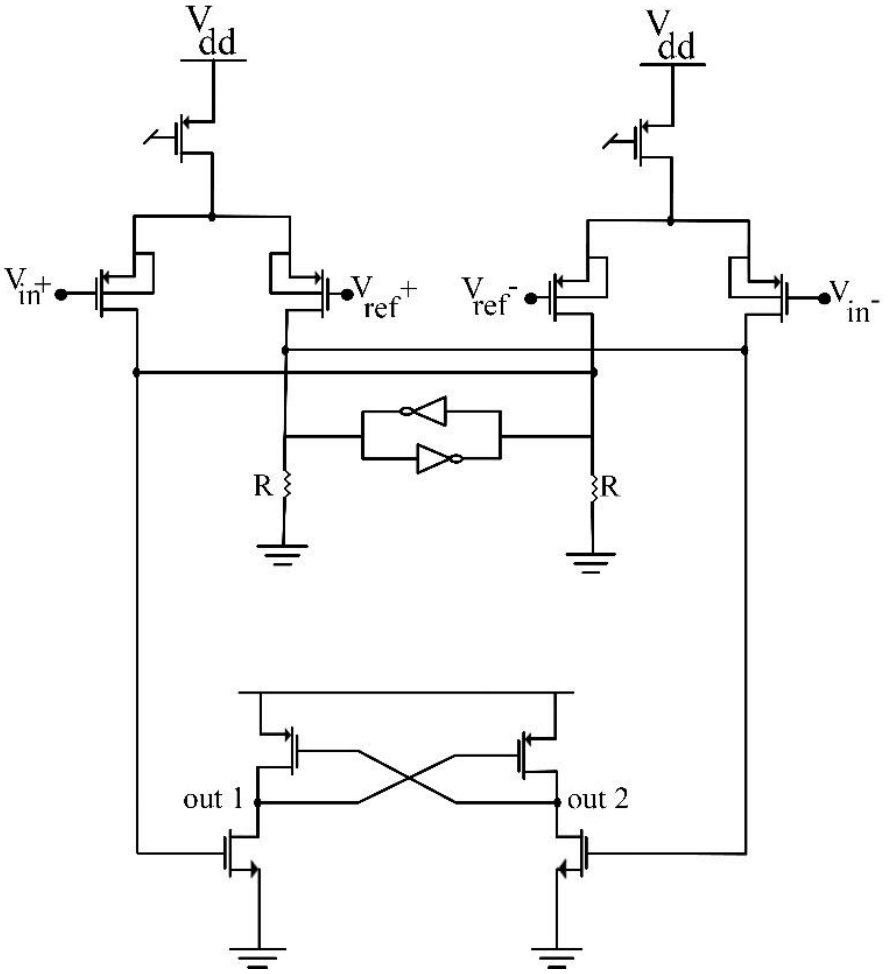

Figure 7. Proposed comparator structure

Also, in the first stage, due to lack of area at the IC level, instead of the passive resistance, active elements are used. That is, the transistors of Figure 7 actually play the role of resistance.

2.2. Buffer

One of the vital blocks is the Buffer block which amplifiers the differential signal (the difference of the main signal from the first stage signal). The transfer of signal by the buffer to the next level at a low and high precision time is one of the problems that, if solved, can take an effective step in ADC speed increase and it can have many applications. For this purpose the structure of Figure 8 is used.

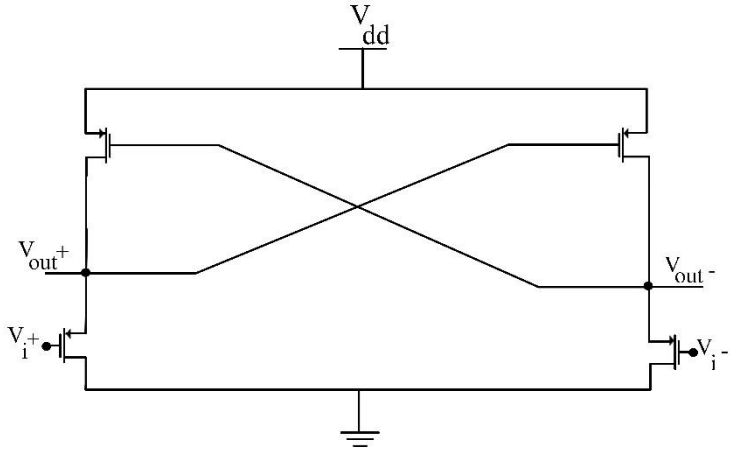

Figure 8. The proposed circuit for the buffer structure

2.3 Amplifier circuit

After extracting the second-stage bits, an amplifier is required to amplify the rest of the signal. 1 ns time is needed to amplify the signal. Looking at the conventional structures of amplifiers with precision, it can be seen that most of these structures use a negative feedback loop. Such amplifiers cannot operate at short time of about 1 ns because of the limitations that Opamp creates. The only solution to achieve an amplified voltage in the short time of 1 ns, is to use an open loop amplifier. The most important issue associated with the use of loop amplifiers is their low accuracy. To solve this problem in the proposed circuit, a method is used to improve this accuracy. For this purpose, the Folded Cascade circuit whose input transistors are scaled is used. This circuit is shown in Figure 9.

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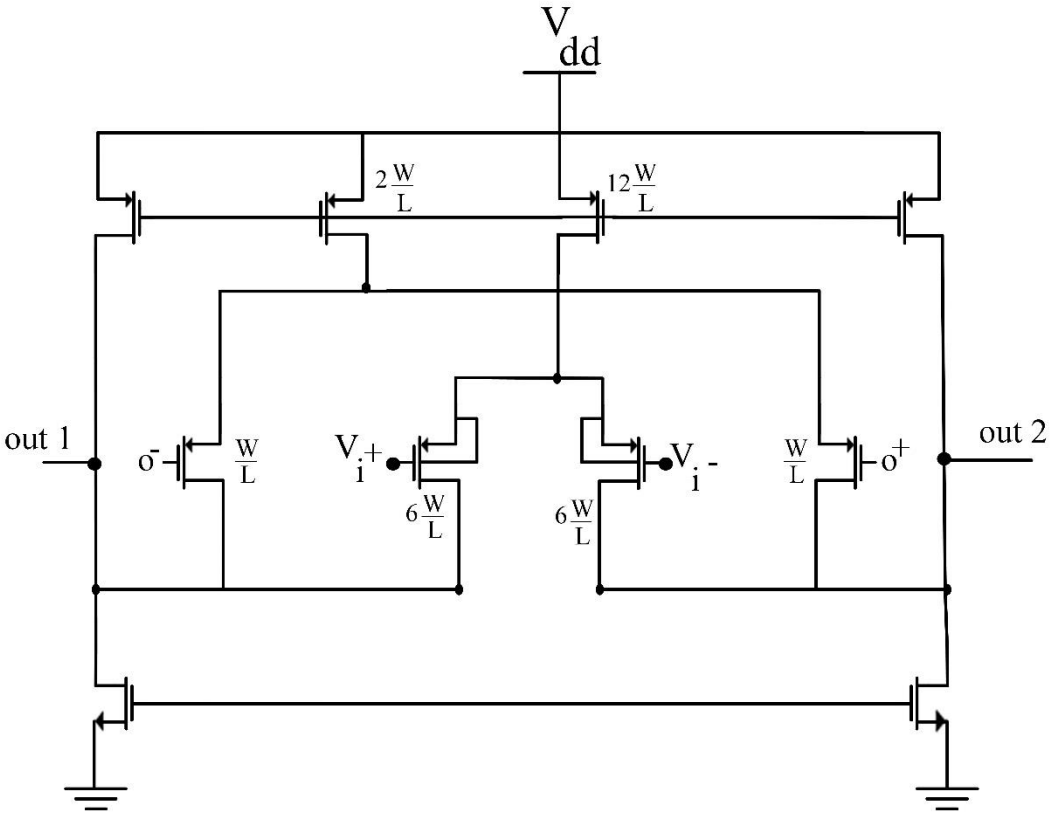

Figure 9. Proposed amplifier structure

2.4. Flash ADC

In this structure, internal convertors are utilized as flash. In this convertor, a series of resistors creates comparative levels and a 2^N-1 comparator circuit compares the input signal with these voltage levels and generates a thermometer code for this signal. Thereafter, this thermometer code is converted to a binary code by a binary conversion circuit. Therefore, in this type of ADCs, the main factor in determining the speed and accuracy of the circuit is the speed and accuracy of the comparator circuits used in the flash. For flash circuits design, we used method of reference [1]. Figure 10 shows the comparator circuit used in flash1. Figure 11 shows the comparator circuit used in flash2,3 and flash4. These comparator circuits consist of three stages, the first stage has the task of amplifying, and the second stage has the task of comparison, and the third stage is latch. On the other hand, the gain of Figure 10 is more than of Figure 11.

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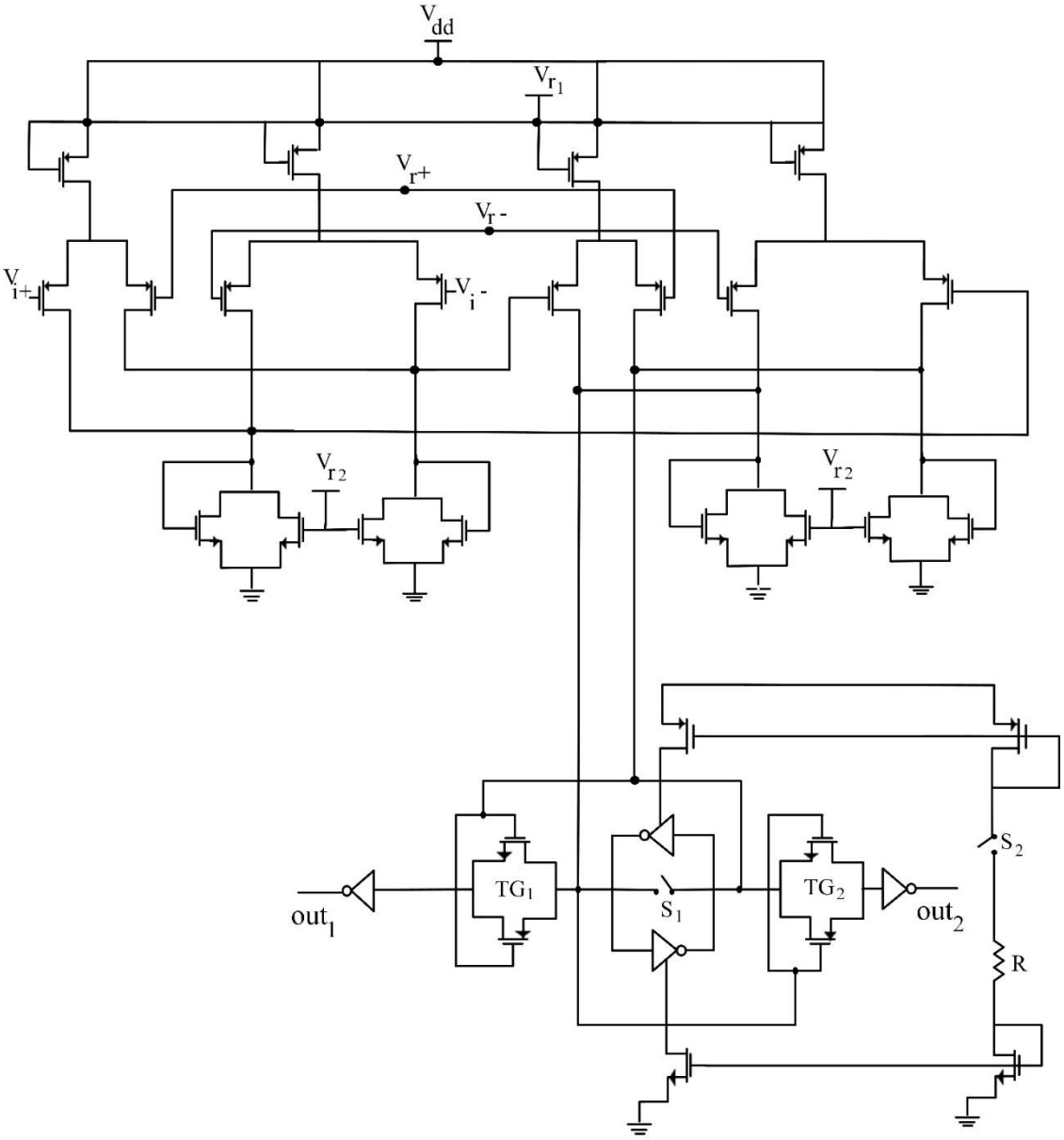

Figure 10. The comparator circuit used in the flash1 [1]

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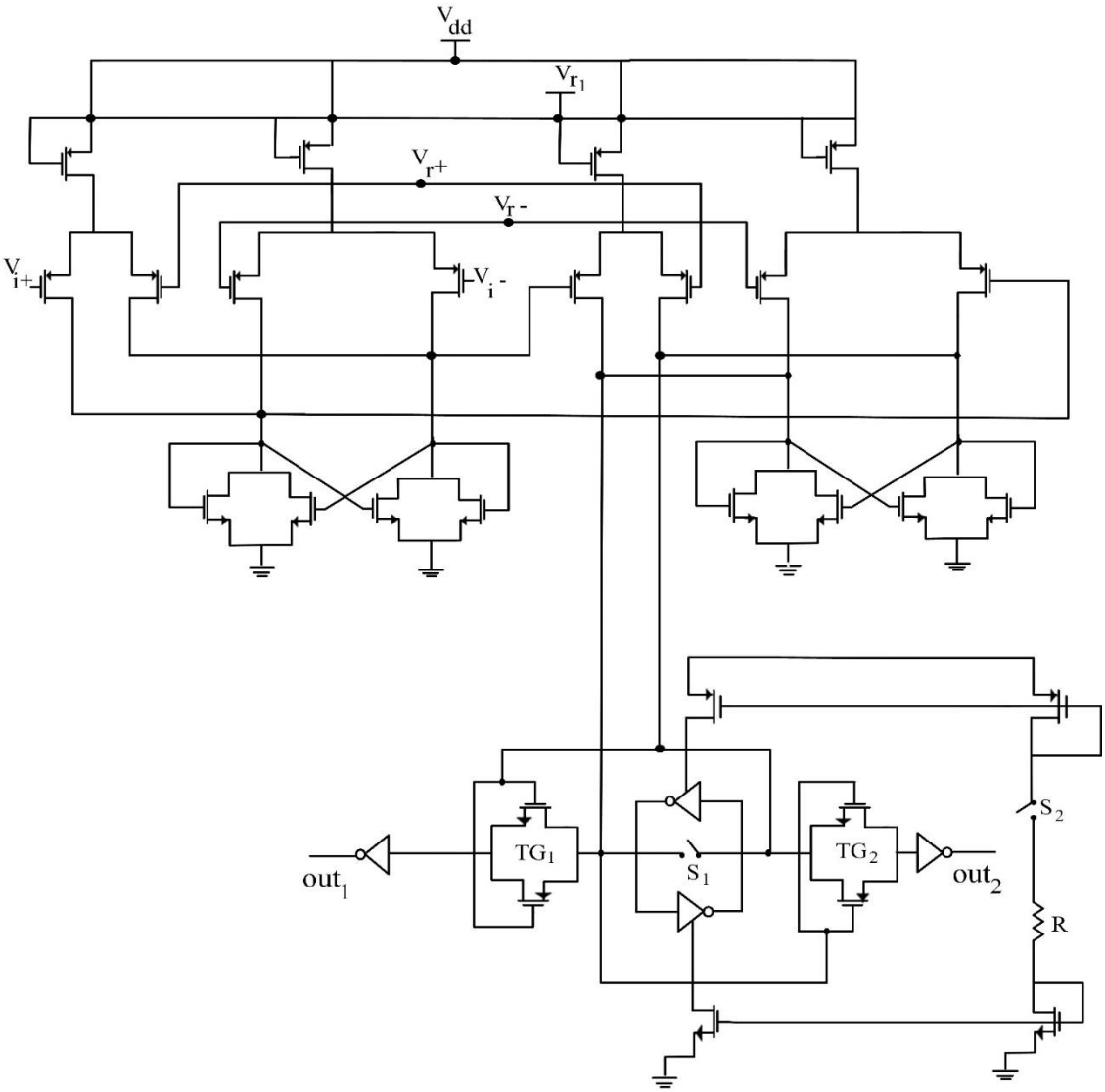

Figure 11. The comparator circuit used in the flash2,3 and flash4 [1]

In order to design binary conversion circuits of flashes, we used method of reference [1], In other words we used 4-bit binary conversion implementation method of reference [1].

2.5. Clock generation circuits

The clock required in ADC is the method of reference [1]. The difference is that, this Ring Counter is made up of two flip-flops to be reset and one flip-flop to be set. On the other hand Ring counter Error Correction Circuit design for two flip-flops. The Ring Counter Error Correction circuit is shown in Figure 12. As in reference [1], In Ring Counter circuit for every clock, one of the outputs (phi0, phi1 and phi2) must be '1' and the rest must be '0'. If this happens otherwise, the error correction circuit will fix it.

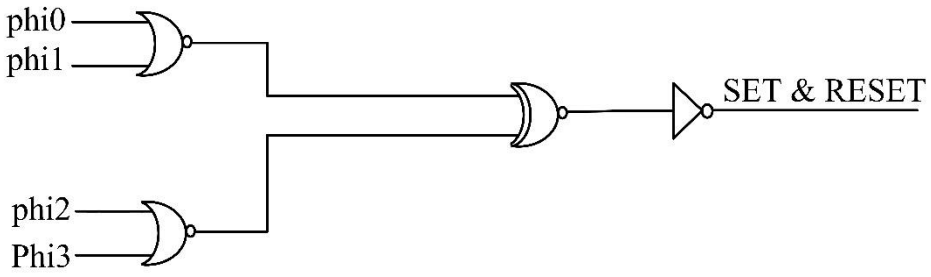

Figure 12. Ring counter Error Correction Circuit [1]

3. Simulation and results

After presenting the final block of the ADC convertor and related circuits which are completely new, this section first presents the simulation results of all circuits separately. Thereafter, the simulation results of the analogue to digital convertor are presented.

3.1. S/H circuit

To bring the simulation results closer to the results of construction, two signals with close frequencies are used. Also if, with this operation, the SNDR output again has values below -80dB, as shown in Figure 13, the proposed circuit for S/H is well suited for the design of an ADC with a sampling rate of 350 MS/s.

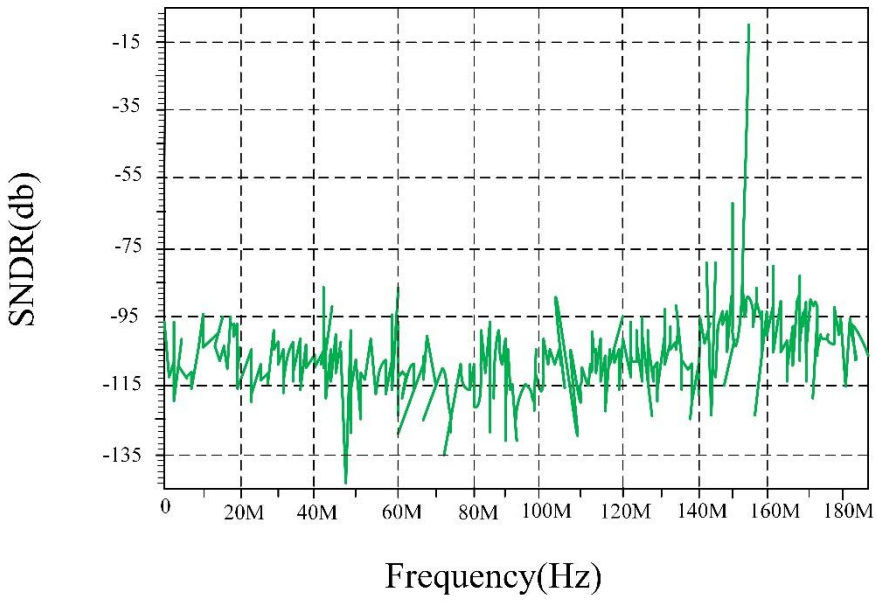

Figure 13. Output of SNDR.

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3.2 Comparator circuit

As previously mentioned the comparator circuit can remove offset, it shown in Figure 14, the circuit offset disappears after several cycles and the circuit operates correctly. Also, based on the simulations carried out, the proposed circuit can detect a voltage difference of 8 mV correctly at a clock frequency of 1 GHz (1 ns period, as shown in Figure 14). If at 1 GHz the comparator circuit can remove offset, then it is certain that it will not develop problem at 350 MHz.

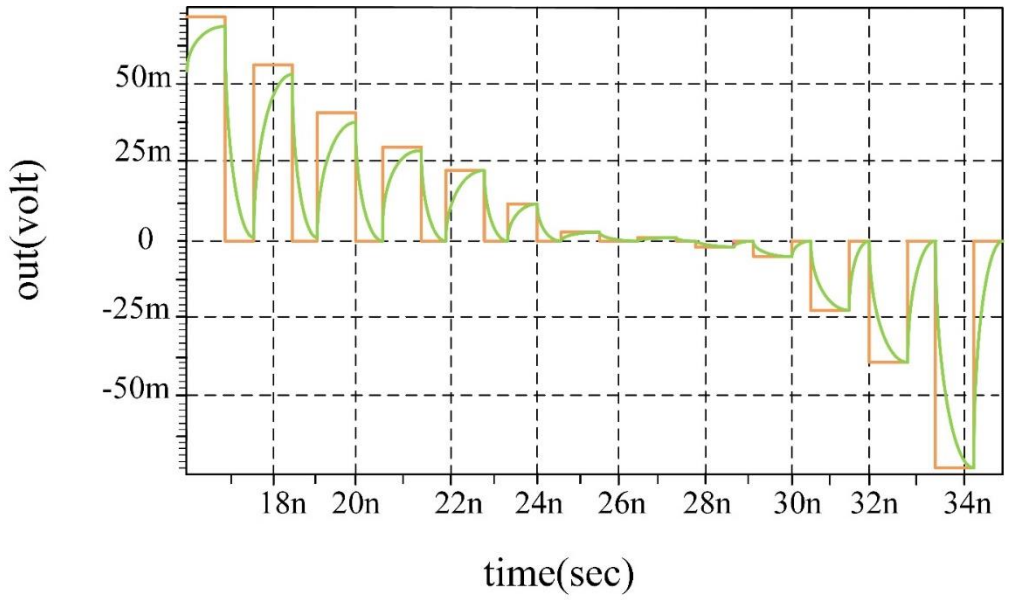

Figure 14. Comparison circuit offset after several cycles

The comparator circuits are tested in the worst conditions, such that a very large positive value is first applied to the comparator, followed by the application of a negative value (up to the LSB/2 level). The comparator should be able to identify this change correctly. In the opposite case, the circuit must correctly detect the change of operation. In Figure 15(a), curves V_{in} are the inputs of Figure 7, and in Figure 15(b), curves output and inverse output are the outputs of Figure 7.

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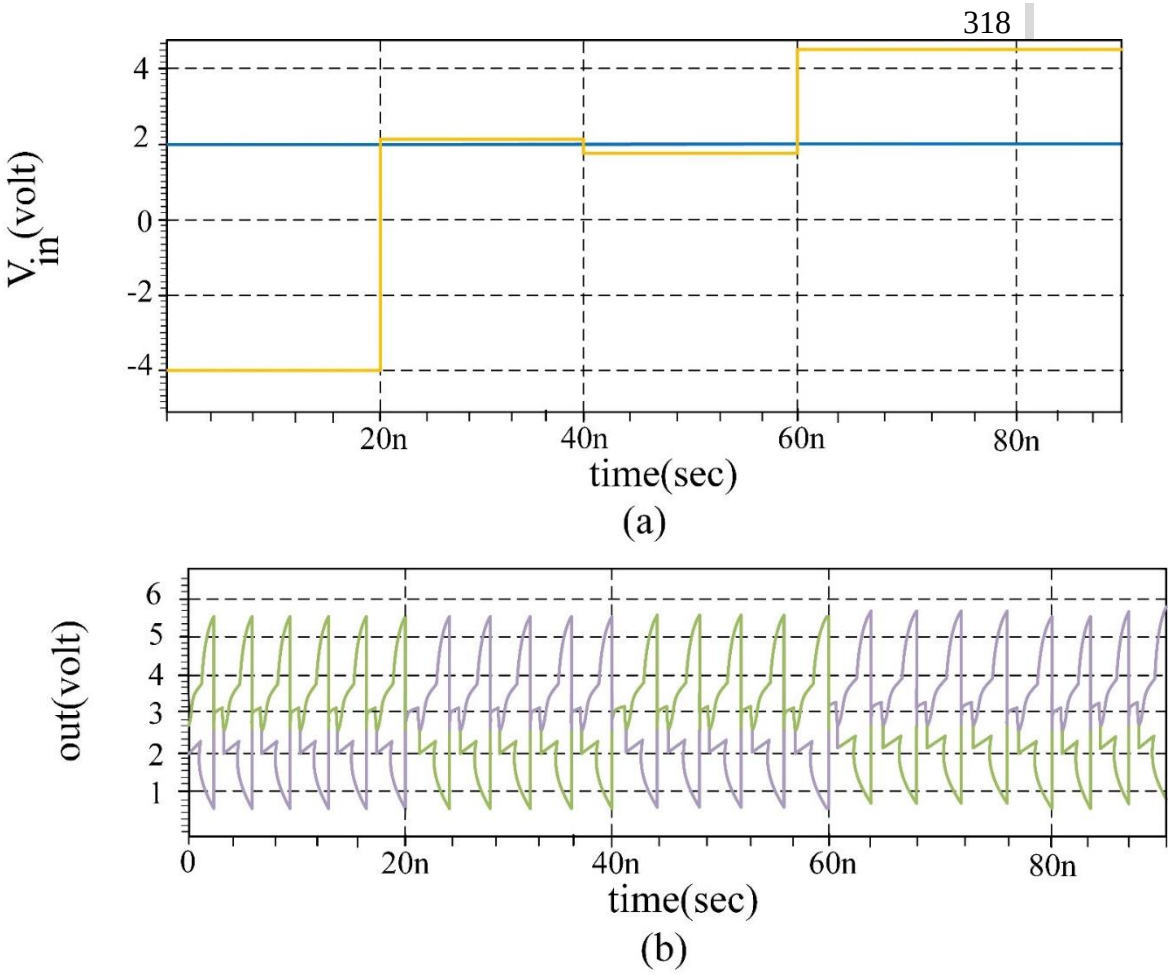

Figure 15. Results of comparator circuit, (a) inputs of Figure7 and (b) outputs of Figure7.

3.3 The buffer circuit

In order to simulate the buffer circuit, a load must be placed on its output. In this study, we considered the load capacitance equal to 1pF.

The proposed buffer (Figure8) has a precision unit rate of 1 GHz (it shown in Figure 16). It is also apparent from the figure that the -3 dB bandwidth is acceptable and can be seen to be above 1 GHz.

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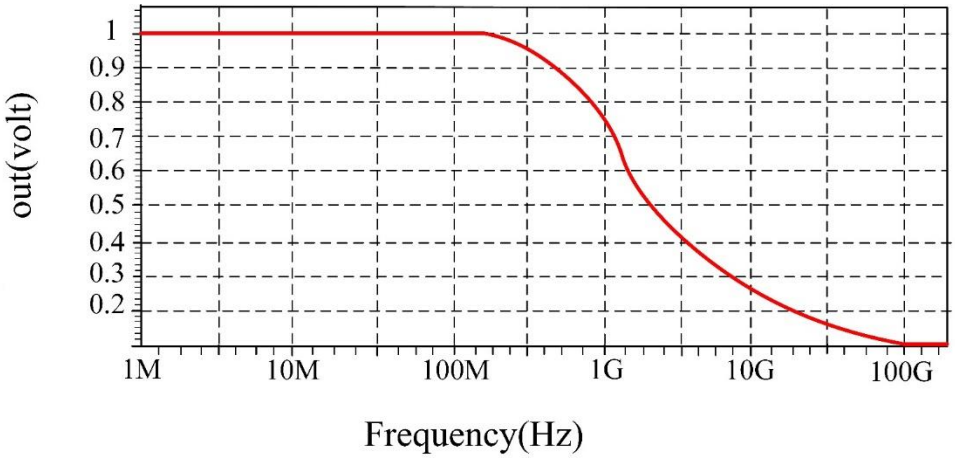
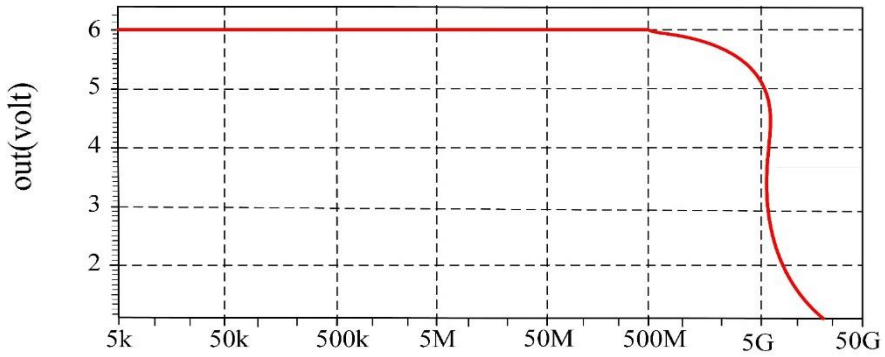


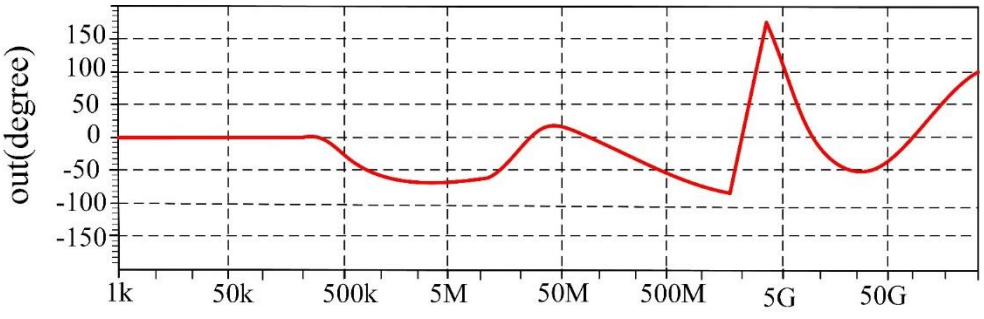
Figure 16. Proposed buffer output (Figure14)

3.4 Amplifier circuit

Figures 17(a) and 17(b) shows the frequency responses of the gain stage (Figure 9) in the second stage. The circuit has a gain of 6V and the bandwidth or -3 dB frequency is 2.58 GHz. The circuit also has better stability because Phase Margin is at a frequency of -3dB equal to 75 degree, which has the best stability The important thing in Figure 17(a) is that the UGB of both stages of the amplifier, where the gain is equal to 1 or 0, is above 10 GHz and this shows the correct performance of the amplifiers.



(a)



(b)

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Figure 17. (a) Gain (out(dB)) for Figure 9 of the second stage and (b) phase response(out(degree)) for Figure 9 of the second stage

3.5. Flash ADC circuits

As mentioned above, for the comparator circuit in flash1 used of Figure10 and for the comparator circuit in flash2,3,4 used of Figure11. These comparator circuits consist of three stages, the first stage has the task of amplifying, and the second stage is the task of comparison, and the third stage is latch, On the other hand, the gain of Figure 10 is more than of Figure 11, which was predicted. The gain of Figure 10 shown at Figure 18 and the gain of Figure 11 shown at Figure 19.

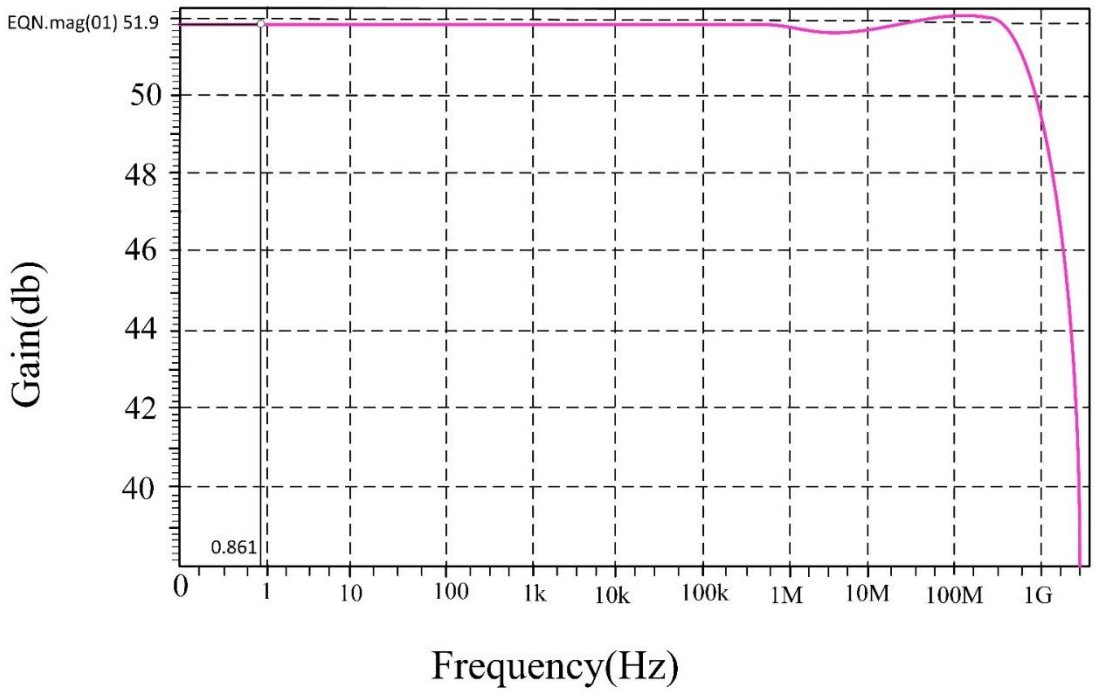

Figure 18. Gain (out (dB)) for Figure 10

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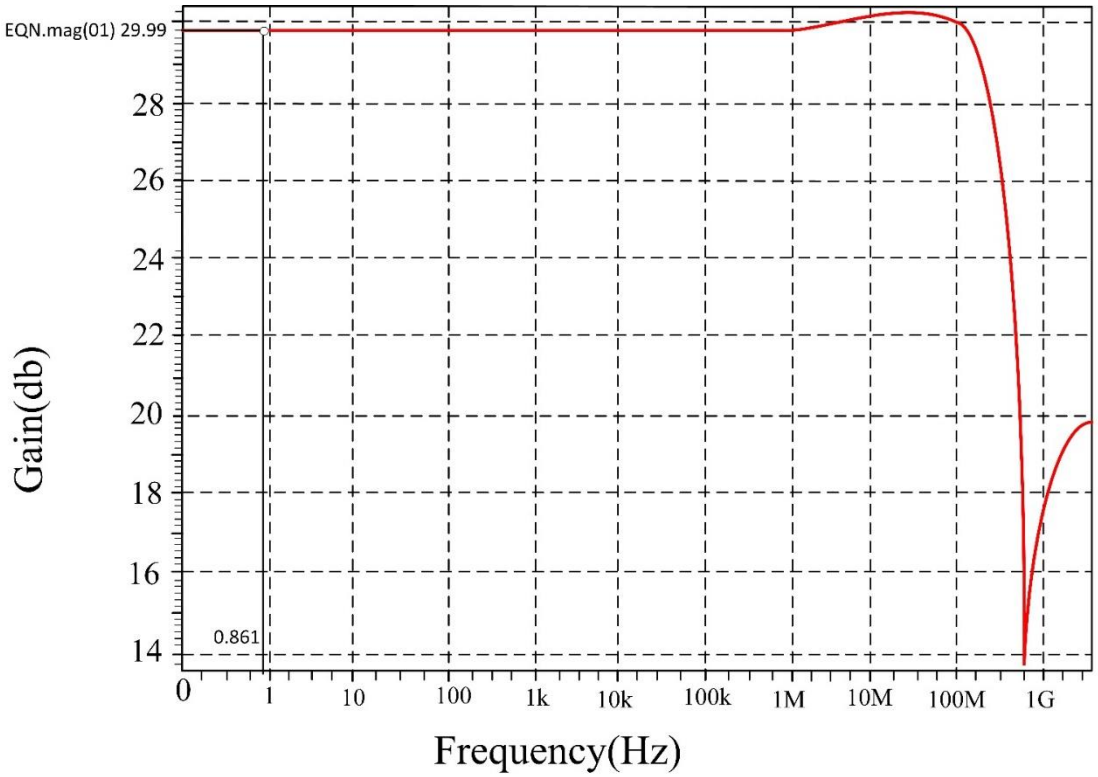
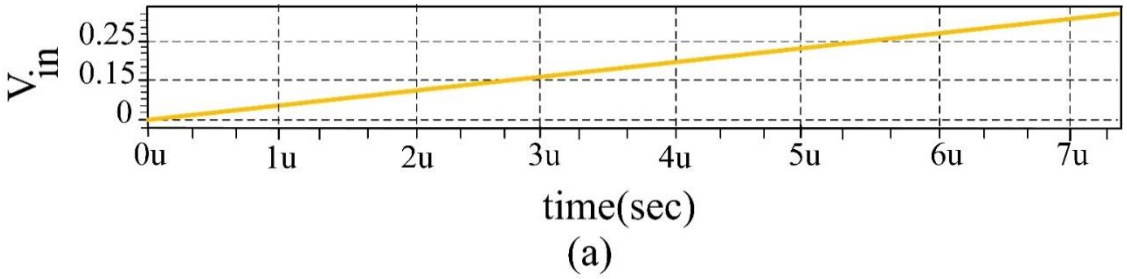


Figure 19. Gain (out (dB)) for Figure 11

The response of one of the 4-bit ADC flashes and the 3-bit ADC flashes as an example to a slope input is shown in Figure 20.



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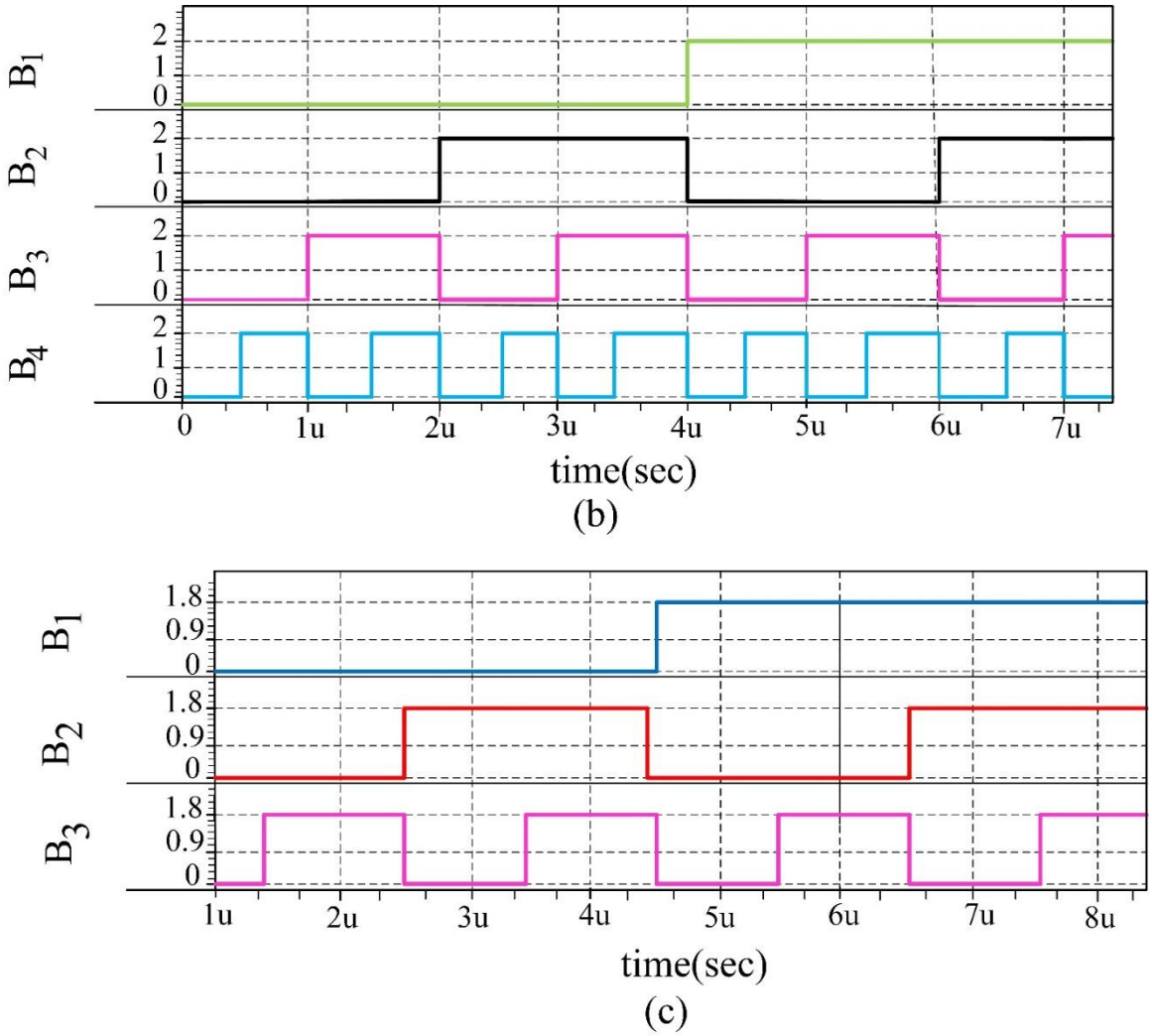

Figure 20. Output of flashes ADC (a) the input signal of 4-bits flash ADC and 3-bits flash, (b) output signals of 4bits flash ADC (B_1, B_2, B_3, B_4) , (c) output signals of 3bits flash ADC (B_1, B_2, B_3)

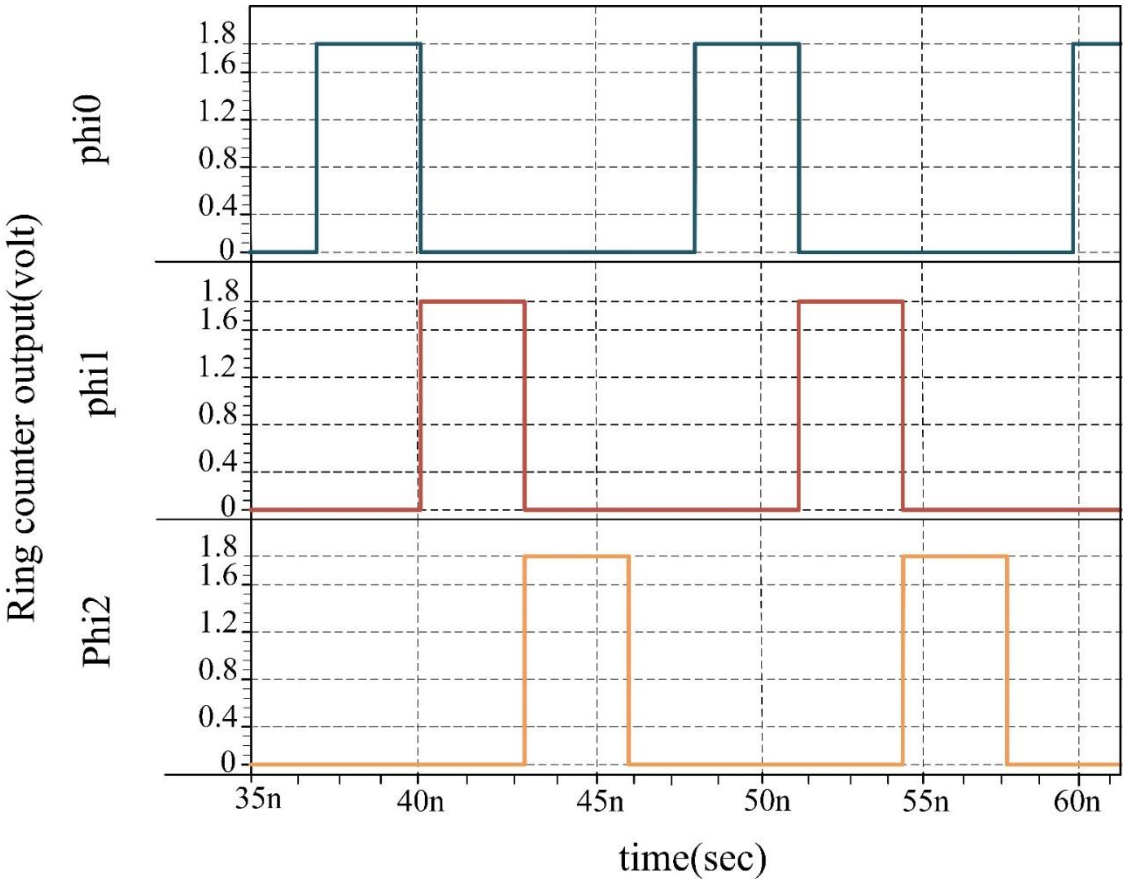

Figure 21. Output of ring counter circuit

4. Conclusion

Since in pipeline analog to digital convertor is disappears about half of conversion time in the amplifier, so in this paper to increase the speed of convertor didn't use the amplifier for the first stage, and to transfer the data from the first stage to the second stage designed a buffer with gain very accurate unit that can transfer the data to the next stage at a low time with high speed and high accuracy. Given the lack of data amplification in first stage, the second stage requires a precision comparator circuit that can detect offset without delay and eliminates it. So a new structure comparator and low power was designed. There is also another idea for further increase of the convertor speed, we designed the analog circuits with open loop structures, and so for the second stage an amplifier with a precision of 6, the open loop was designed. A new error correction circuit was designed for the Ring Counter. Since it is necessary for a 10-bit Pipeline ADC to have the S/H circuit having a minimum accuracy of 11 bits. Therefore,

the S/H circuit designed has a precision above 11 bits. A 10-bit pipeline convertor with sampling speed of 350 MS/s with 0.18 µm TSMC technology was designed and simulated in this study. All internal circuits of this convertor were designed and their simulation results were presented separately. Finally, the overall simulation of the ADC convertor was carried out and the results of the proposed simulation were: 10-bit resolution, sampling rate of 350 MS/s and power consumption of 75mW. All analyzes were also performed using the Hspice software in the 0.18 µm process. In Table 1, the simulation results are compared with previous study.

Table 1 comparison of the proposed ADC with previous work.

Speed (MHz)	Power (mW)	SNDR (dB)	SFDR (dB)	Bit	Process (um)	Year	Ref
100	19.7	54.4	-	10	0.18	2018	[1]
50	0.826	57	61.8	10	0.13	2010	[17]
1000	1200	69	86	14	0.065	2014	[22]
500	950	52	78	14	0.18	2015	[23]
250	49.7	67	84.6	12	0.065	2015	[24]
250	120	74.4	87.1	14	0.018	2018	[25]
166	38.9	45.9	50	8	0.018	2017	[27]
250	28	61.84	78.2	10	0.018	2017	[28]
350	75	60.52	69.27	10	0.18	2018	This Work

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